Lecture 7

Synchronous Sequential Logic

Outline

- Sequential Circuits
- Latches
- Flip-Flops

Sequential Circuits

- Consist of a combinational circuit to which storage elements are connected to form a feedback path
- State . the state of the memory devices now, also called **current state**
- Next states and outputs are functions of inputs and present states of storage elements

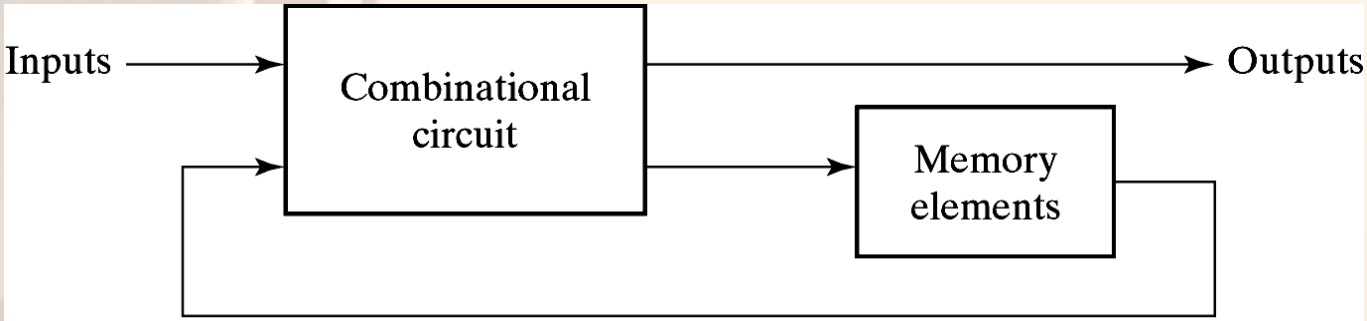
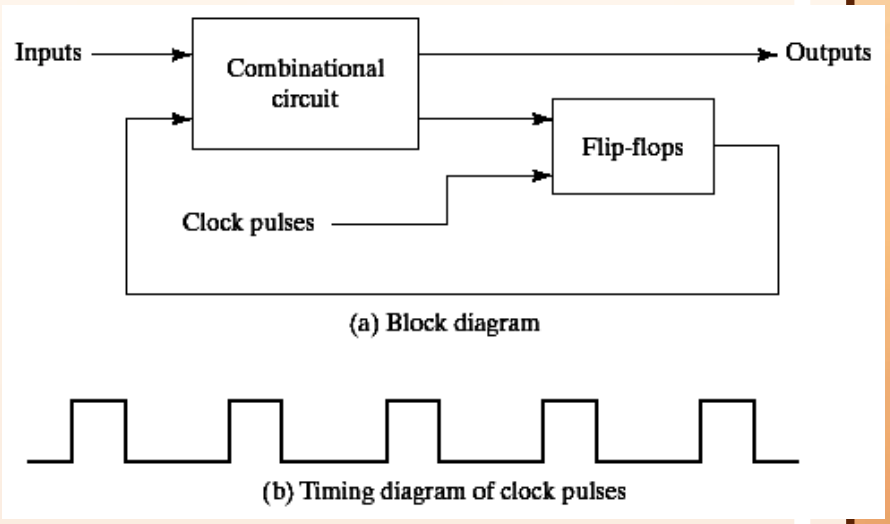


Fig. 5-1 Block Diagram of Sequential Circuit

Two Types of Sequential Circuits

- Asynchronous sequential circuit
  - Depends upon the input signals at **any instant of time and** their change order
  - May have better performance but hard to design

- Synchronous sequential circuit
  - Defined from the knowledge of its signals at **discrete instants of time**
  - Much easier to design (preferred design style)
  - Synchronized by a periodic train of clock pulses



Memory Elements

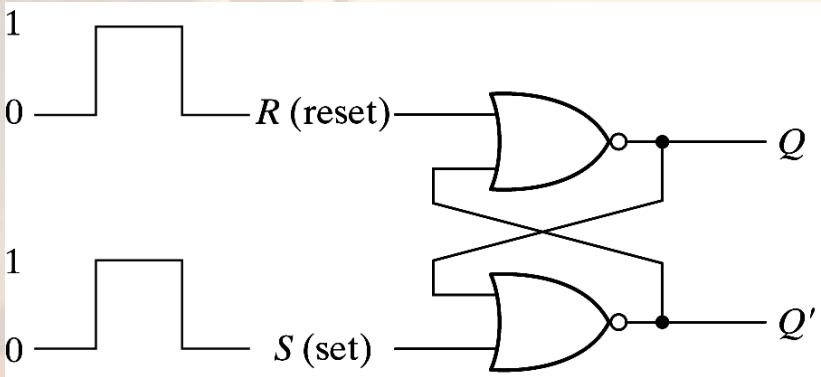
- Allow sequential logic design
- Latch . a level-sensitive memory element
  - SR latches
  - D latches
- Flip-Flop . an edge-triggered memory element
  - Master-slave flip-flop
  - Edge-triggered flip-flop
- RAM and ROM . a mass memory element

Latches

- The most basic types of flip-flops operate with signal levels
- The basic circuits from which all flip-flops are constructed
- Useful for storing binary information and for the design of asynchronous sequential circuits
  - Not practical for use in synchronous sequential circuits
  - Avoid to use latches as possible in synchronous sequential circuits to avoid design problems

SR Latch

- A circuit with two cross-coupled NOR gates or two cross-coupled NAND gates
- Two useful states:
  - S=1, R=0 " set state (Q will become to 1)
  - S=0, R=1 " reset state (Q will become to 0)
- When S=0 and R=0 " keep the current value

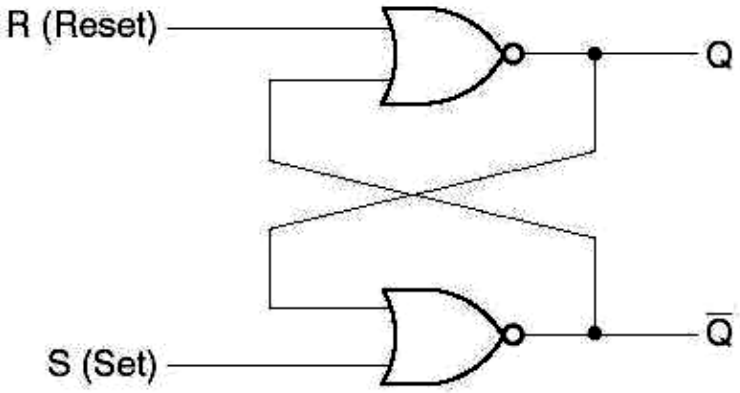


(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	

(b) Function table

Undefined State in SR Latch



(a) Logic diagram

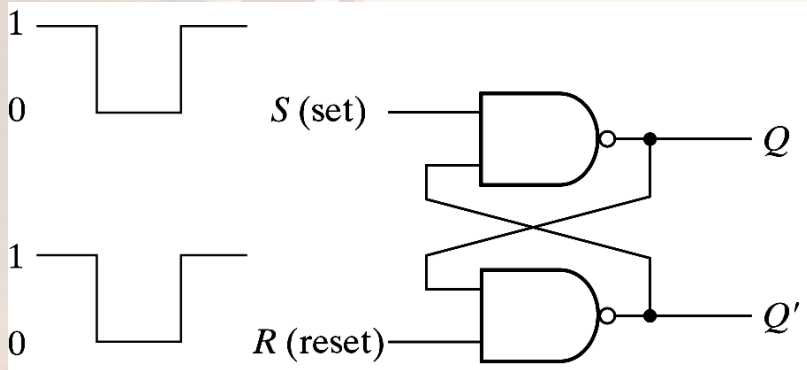
S	R	Q	$\overline{Q}$	
1	0	1	0	Set state
0	0	1	0	
0	1	0	1	Reset state
0	0	0	1	
1	1	0	0	Undefined

(b) Function table

Should be very careful for this case

SR Latch with NAND Gates

- The SR latches constructed with two cross-coupled NAND gates are **active-low**
  - S=1, R=0 " reset state (Q will become to 0)
  - S=0, R=1 " set state (Q will become to 1)
  - S=1, R=1 " unchanged



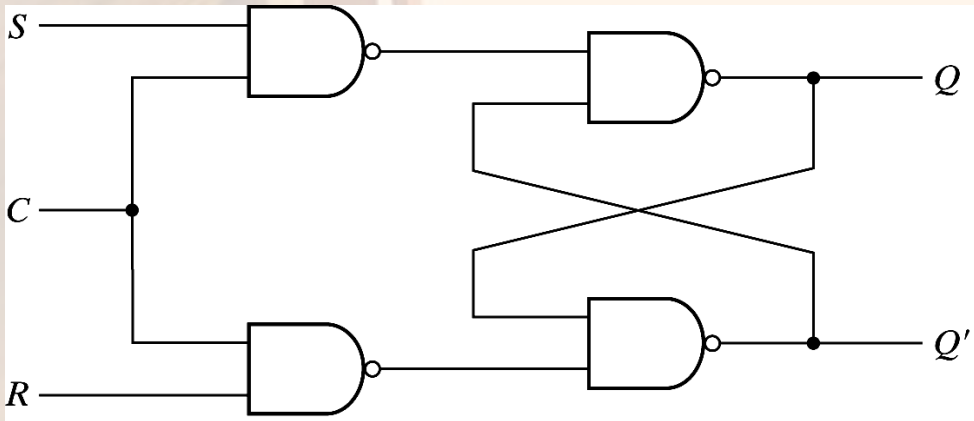
S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	

(a) Logic diagram (b) Function table

Fig. 5-4 *SR* Latch with NAND Gates

SR Latch with Control Input

- Add an additional control input to determine when the state of the latch can be changed
- C=0: S and R are disabled (no change at outputs)
- C=1: S and R are active-high



(a) Logic diagram

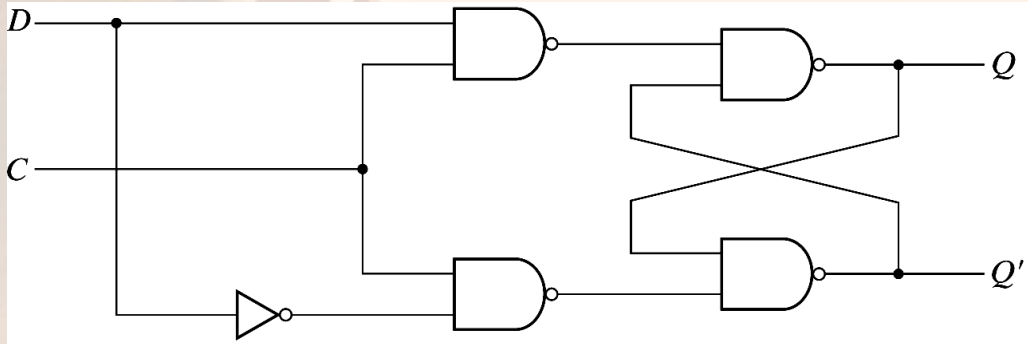
C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; Reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

(b) Function table

Fig. 5-5 SR Latch with Control Input

D Latch

- D latch has only two inputs: D(data) and C(control)
  - Use the value of D to set the output value
  - Eliminate the indeterminate state in the SR latches
- The D input goes directly to the S input and its complement is applied to the R input
  - D=1 → Q=1 → S=1, R=0



(a) Logic diagram

C	D	Next state of Q
0	X	No change
1	0	Q = 0; Reset state
1	1	Q = 1; Set state

(b) Function table

Fig. 5-6 D Latch

Graphic Symbols for Latches

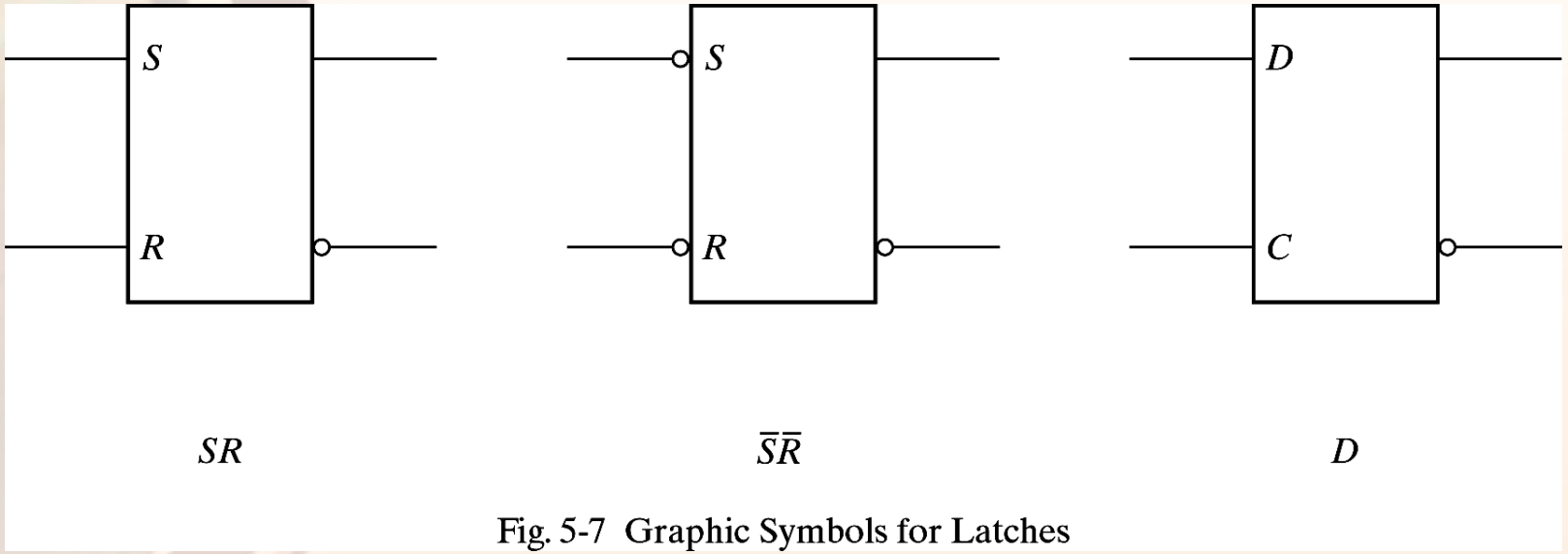


Fig. 5-7 Graphic Symbols for Latches

Flip-Flops

- The state of a latch or flip-flop is switched by a change in the control input
- This momentary change is called a **trigger**
- Latch: level-sensitive
- Flip-Flop: edge-triggered

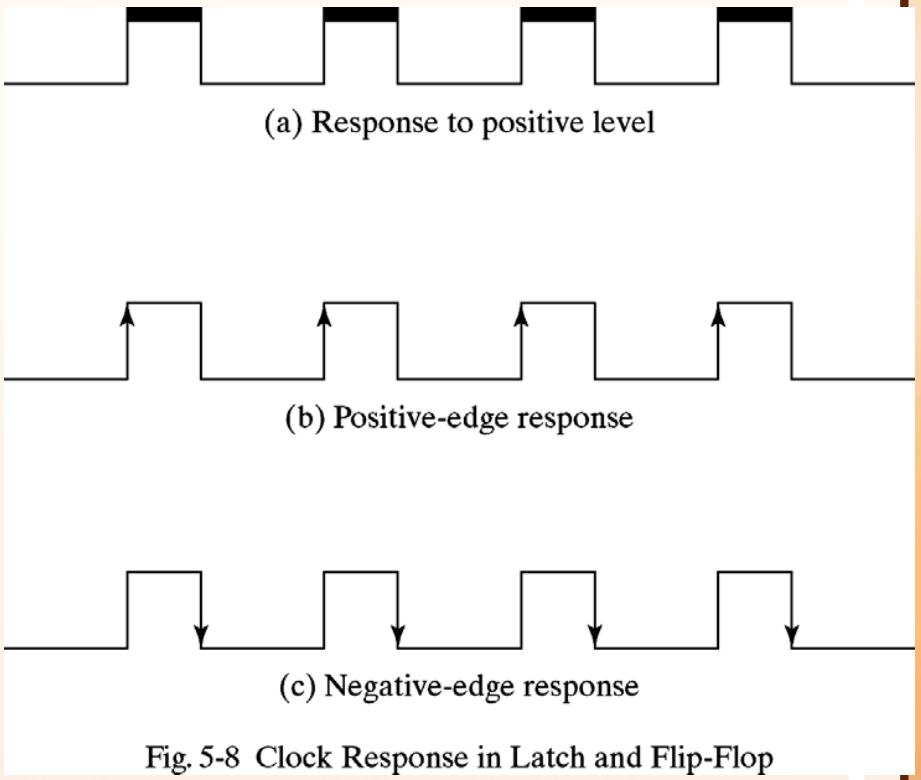
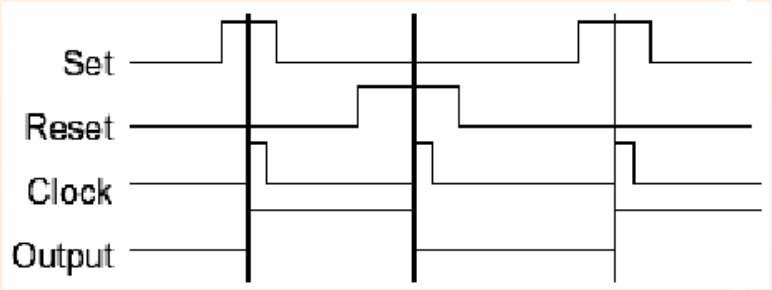


Fig. 5-8 Clock Response in Latch and Flip-Flop

Latch vs. Flip-Flop

- Latch:
  - Change stored value under specific status of the control signals
  - Transparent for input signals when control signal is .on.
  - May cause combinational feedback loop and extra changes at the output

- Flip-Flop:
  - Can only change stored value by a momentary switch in value of the control signals
  - Cannot .see. the change of its output in the same clock pulse
  - Encounter fewer problems than using latches



reading

- M. Morris Mano , Michael D. Ciletti “Digital Design With an Introduction to the Verilog HDL” FIFTH EDITION
  - Sections: 5.1 to 5.4